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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,920	09/11/2003	Raymond S. Tetrick	884.A31US2	6016

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EXAMINER	
BRAGDON, REGINALD GLENWOOD	

ART UNIT	PAPER NUMBER
2188	

DATE MAILED: 06/17/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/659,920	TETRICK, RAYMOND S.	
	Examiner	Art Unit	
	Reginald G. Bragdon	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-40* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *34-40* is/are allowed.

6)☒ Claim(s) *21-24 and 26-32* is/are rejected.

7)☒ Claim(s) *25 and 33* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 28-33 are objected to because of the following informalities:

As per claim 28, line 7, "continues" should be --continuing--.

As per claim 28, line 8, "stops" should be --stopping--.

All dependent claims are objected to as having the same deficiencies as the claims they depend from.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-24 and 26-32 are rejected under 35 U.S.C. 102(b) as being anticipated by Macon, Jr. et al. (5,600,817).

As per claim 21, Macon, Jr. et al. teaches a read-ahead ("*prefetch*") process for a mass storage ("*input/output device*") system. A portion of a cache in the main memory (DCACHE 7) is set aside as a "Most Recently Read-Ahead Section" or MRRS. The system includes a file system 10 ("*I/O control circuit*"), which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address

12, and CONT 18) ("*a prefetch circuit to prefetch a data block into the memory in advance of a subsequent read from the I/O device*"). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) represents the "predicted address", and data is prefetched for this address value. See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("*wherein the subsequent read is tracked to determine if the subsequent read reads from the predicted address*"). See column 5, lines 11-17, and column 7, lines 37-39. Macon, Jr. et al. further teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS in step B) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O") ("*the prefetch circuit is adapted perform at least one of to...stop prefetching in response to the subsequent read*").

As per claim 22, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 23, the read ahead functionality is located within the file system 10 which corresponds to the claimed "*I/O control circuit*" as detailed above.

As per claim 24, the file system, in which the read ahead functionality resides, is an interface for main memory 3, CPU 2, and mass storage 4.

As per claim 26, Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted

address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G").

As per claim 27, Macon, Jr. et al. teaches, with reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O").

As per claim 28, Macon, Jr. et al. teaches a CPU 2 ("*a processor*") and a mass storage 4 ("*an Input/Output (I/O) device*"). The system includes a file system 10, which may be embodied in hardware or software. See column 4, lines 43-51. The file system includes read-ahead functionality (Length 16, COMP 14, Address 12, and CONT 18). The address value A1 represents the "preceding address" upon which the predicted prefetch address is based (in that the read precedes the prefetching). See column 7, lines 30-32. The address value A2 (derived from A1+L, the number of units to prefetch value) is used to prefetch data ("*the prefetch interface predicts an address needed within the I/O device to satisfy the request*"). See column 7, lines 32-34. The address value A2 is stored in the MRRS. See column 7, line 36. When an next address is "demanded", the address is compared to the address (in this case A2) associated with the MRRS ("*the prefetch interface tracks its performance*"). See column 5, lines 11-17, and column 7, lines 37-39. Macon, Jr. et al. teaches, with reference to figure 6, that as long as there is a first hit in the MRRS (step "B", where the address value in the MRRS is the predicted address and a hit represents the demand address matching the address in the MRRS as set forth in column 5, lines 48-50), then prefetching of a number L of units continues (step "G") ("*performs at least one of, in response to success rates, continuing to prefetch for additional data and stopping prefetching for the additional data*"). Macon, Jr. et al. further teaches, with

reference to figure 6, that if there is a MRRS miss (i.e. the demand address does not match the value in the MRRS) and a DCACHE hit (step "I"), no prefetching occurs (processing goes to step "O") ("*performs at least one of, in response to success rates, continuing to prefetch for additional data and stopping prefetching for the additional data*"). The MRRS is representative of prior prefetched data (most recently read ahead section), where a first hit in the MRRS results in further prefetching.

As per claim 29, Macon, Jr. et al. teaches that the entire address value in the MRRS must match the demand value (column 5, lines 48-50). Therefore, "at least a portion of the prefetched data" satisfies the request.

As per claim 30, as set forth in figure 6, the prefetching is configured to adjust whether or not to prefetch, and how much to prefetch (the L value) based on hits or misses in the MRRS and Dcache.

As per claim 31, CONT 18 represents a state machine, and it performs the function of updating, or adjusting, the MRRS value and the length 16 value. See column 5, lines 20-47.

As per claim 32, CONT 18 controls whether prefetching occurs (i.e. step G of figure 6 is performed) or does not occur (step G is not performed). See figure 6.

Allowable Subject Matter

4. Claims 34-40 are allowed.

5. Claims 25 and 33 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

6. Applicant's arguments filed 20 May 2005 have been fully considered but they are not persuasive.

Applicant argues that Macon, Jr. et al. always performs a prefetch into cache for each piece of data and that the amended claims now recited that for at least some blocks, prefetching does not occur.

With respect to claim 21, Applicant example on page 6, showing how "Macon always performs at least one prefetch for a given entry" does not fully encompass the teachings of figure 6. Applicant's example includes step F shown in figure 6 of Macon, Jr. et al. As set forth by the Examiner in the rejection of claim 21, the path followed through figure 6 is steps A, B, I, J, K and O. In this path there is no prefetching performed. And, contrary to Applicant's assertion, the amended claim language of claim 21 does not convey "for at least some blocks, prefetching does not occur". The limitation of "[performing] at least one of to continue prefetching in response to the subsequent read" can be interpreted as setting forth instances in which prefetching always continues in response to the subsequent read (i.e. Applicant has not claimed when to continue prefetching and when to stop prefetching).

With respect to claim 28, the amended claim language does not convey "for at least some blocks, prefetching does not occur". The limitation of "[performing] at least one of to continue prefetching in response to the subsequent read" can be interpreted as setting forth instances in which prefetching always continues in response to the subsequent read (i.e. Applicant has not claimed when to continue prefetching and when to stop prefetching). And as noted above for claim 21, the flowchart of figure 6 shows a path which does not include performing step F.

Conclusion

7. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks
Washington, D.C. 20231

All "OFFICIAL" patent application related correspondence transmitted by FAX must be directed to the central FAX number at **(703) 872-9306**:

"INFORMAL" or "DRAFT" FAX communications may be sent to the Examiner at **(571) 273-4204**, only after approval by the Examiner.

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA., Fourth Floor (receptionist).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Reginald G. Bragdon whose telephone number is (571) 272-4204. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and every other Friday from 7:00 AM to 3:30 PM.

The examiner's supervisor, Mano Padmanabhan, can be reached at (571) 272-4210.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Reginald G. Bragdon
Primary Patent Examiner
Art Unit 2188

RGB
June 16, 2005